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Intelligence Partitioning and Data Reduction in Wireless Visual Sensor Networks

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Abstract:

Wireless Visual Sensor Network (WVSN) is formed by deploying many Visual Sensor Nodes (VSNs) in the field. The individual VSN contains an image sensor, on board processor, storage capacity, energy resource and wireless communication link. In comparison to the traditional wireless sensor networks, which operate on one dimensional data, the WVSN operates on two dimensional data which requires fast processing unit and large communication bandwidth. The research focus within the field of WVSN has been on the two extremes, involving either sending raw compressed data to the Central Base Station (CBS) without local processing or conducting all processing locally at the VSN and transmitting only the final results.

The research work in this thesis focuses on balancing the processing load between hardware and software implementation at the VSN as well as partitioning tasks between local and central processing. The lifetime of the VSN is predicted by evaluating the energy requirement of the embedded platform with a combination of a Field Programmable Gate Array (FPGA) and a microcontroller for the implementation of the VSN. The main contribution of this thesis includes the exploration of the intelligence partitioning strategies between VSN and the CBS as well as the architecture for the implementation of the VSN. Based on the proposed architecture, the various data reduction techniques such as image coding change coding and Region of Interest (ROI) coding are explored for reducing the output data and, ultimately, reducing the energy consumption of each of the VSN. The effect of packets receiving/forwarding and node density in a multi-hop network on implementation issues of the VSN has also been explored.

Advancements in FPGAs have been the motivation behind their choice as the vision processing platform for implementing the VSN. This choice is based on its reduced time-to-market, low Non-Recurring Engineering (NRE) cost and programmability as compared to Application Specific Integrated Circuits (ASICs). The other part of the architecture of the VSN is the Sentio32 platform, which is used for vision processing in the software implementation and for communicating the results in the hardware implementation.

Results show that the intelligence partitioning strategy in which the pixel based image processing tasks are performed using FPGA and the compressed results are transmitted to the CBS for further processing, is the best strategy. For compressing the data at the VSN, the best approach is to use CCITT Group 4 compression method in combination with change coding and ROI coding. The selected intelligence partitioning strategy reduces the computation energy consumption and the compression approach reduces the communication energy consumption. The overall effect is the reduced total energy consumption, which increases the lifetime of the VSN.